



THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:
Haitham H. AKKARY et al.

Appl. No: 10/724,863

Confirmation No: 1592

Filed: December 2, 2003

For: SINGLE-VERSION DATA CACHE
WITH MULTIPLE CHECKPOINT
SUPPORT

Art Unit: 2186

Examiner: Not Yet Assigned

Atty. Docket No: 42339-193270

Customer No:

26694

PATENT TRADEMARK OFFICE

Information Disclosure Statement

Commissioner for Patents
P.O. Box 1450
Alexandria, Va. 22313-1450

Sir:

This is an Information Disclosure Statement submitted under 37 C.F.R. § 1.97 within the time specified under 37 C.F.R. § 1.97(b).

In order to comply with applicant's duty of disclosure under 37 C.F.R. § 1.56, the U.S. Patent and Trademark Office is notified of the documents which are listed on the attached Form PTO/SB/08A and which the Examiner may deem relevant to patentability of the claims of the above-identified application. One copy of each of the listed documents is submitted herewith.

The present Information Disclosure Statement is being filed before the mailing date of the first Office Action on the merits, and therefore no Statement Under 37 C.F.R. § 1.97(e) or fee under 37 C.F.R. § 1.17(p) is required.

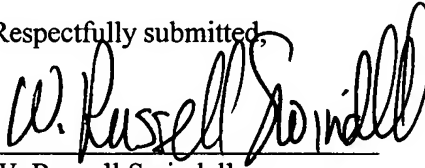
Applicants: Haitham H. AKKARY et al.
Attorney's Doc. No. 42339-193270

In view of the above, no further translation or statement of relevance is required, and as all requirements of 37 C.F.R. § 1.97 and all official guide lines pertaining to Information Disclosure Statements have been complied with, and it is therefore respectfully requested that the Examiner consider the documents and make them of record.

Please charge any necessary fee or credit any overpayment in connection with this Information Disclosure Statement to Deposit Account No. 22-0261.

Date: 4/20/07

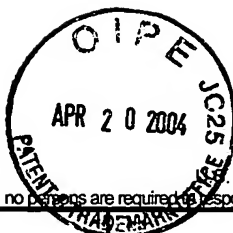
Respectfully submitted,



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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 1 of 2

Complete if Known

Application Number	10/724,863
Filing Date	December 2, 2003
First Named Inventor	Haitham H. AKKARY et al.
Group Art Unit	2181
Examiner Name	Not Yet Assigned
Attorney Docket Number	42339-193270

U.S. PATENT DOCUMENTS

Examiner Initials *	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code ² (if known)			
	A1	6,591,342	B1	AKKARY et al.	07-08-2003	

FOREIGN PATENT DOCUMENTS

Examiner Initials *	Cite No. ¹	Foreign Patent Document			Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ₈
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✓	A2	BALASUBRAMONIAN et al., "Reducing the Complexity of the Register File in Dynamic Superscalar Processors", In <i>Proceedings of the 34th International Symposium on Microarchitecture</i> , Dec. 2001, pgs. 237-248.	
✓	A3	BREKELBAUM et al., "Hierarchical Scheduling Windows", In <i>Proceedings of the 35th International Symposium on Microarchitecture</i> , Nov. 2002, pgs. 27-36.	
✓	A4	BROWN et al., "Select-Free Instruction Scheduling Logic", In <i>Proceedings of the 34th International Symposium on Microarchitecture</i> , Dec. 2001, pgs. 204-213.	
✓	A5	ZALAMEA et al., "Two-level Hierarchical Register File Organization for VLIW Processors", In <i>Proceedings of the 33rd International Symposium on Microarchitecture</i> , Dec. 2000, pgs. 137-146.	
✓	A6	CANAL et al., "A Low-Complexity Issue Logic", In <i>Proceedings of the 2000 International Conference on Supercomputing</i> , Jun. 2000, pgs. 327-335.	
✓	A7	CAPITANIO et al., "Partitioned Register Files for VLIWs: A Preliminary Analysis of Tradeoffs", In <i>Proceedings of the 25th Int'l Symposium on Microarchitecture</i> , Dec. 1992, pgs. 292-300.	
✓	A8	GOPAL et al., "Speculative Versioning Cache", In <i>Proceedings of the Fourth International Symposium on High-Performance Computer Architecture</i> , Feb. 1998, pgs 195-205.	
✓	A9	HAMMOND et al., "Data Speculation Support for a Chip Multiprocessor", In <i>Proceedings of the Eighth Symposium on Architectural Support for Programming Languages and Operating Systems</i> , Oct. 1998, pgs. 58-69.	
✓	A10	HENRY et al., "Circuits for Wide-Window Superscalar Processors", In <i>Proceedings of the 27th Annual International Symposium on Computer Architecture</i> , June 2000, pgs. 236-247.	
✓	A11	HINTON et al., "The Microarchitecture of the Pentium ® 4 Processor", <i>Intel Technology Journal</i> Q1, Feb. 2001, pgs. 1-13.	
✓	A12	JACOBSEN et al., "Assigning Confidence to Conditional Branch Predictions", In <i>Proceedings of the 29th International Symposium on Microarchitecture</i> , Dec. 1996, pgs. 142-152.	
✓	A13	KARKHANIS et al., "A Day in the Life of a Data Cache Miss", In <i>Workshop on Memory Performance Issues</i> , 2002, pgs. 1-10.	
✓	A14	KNIGHT, "An Architecture for Mostly Functional Languages", In <i>Proceedings of ACM Lisp and Functional Programming Conference</i> , Aug. 1986, pgs. 500-519 (reprint pgs. 105-112).	

✓	A15	LEBECK et al., "A Large, Fast Instruction Window for Tolerating Cache Misses", In <i>Proceedings of the 29th Annual International Symposium on Computer Architecture</i> , May 2002, pgs. 59-70.	
✓	A16	LEIBHOLZ et al., "The Alpha 21264: A 500 MHz Out-of-Order Execution Microprocessor", In <i>Proceedings of the 42nd IEEE Computer Society International Conference (COMPCON)</i> , Feb. 1997, pgs. 28-36	
✓	A17	MARTÍNEZ et al., "Cherry: Checkpointed Early Resource Recycling in Out-of-order Microprocessors", In <i>Proceedings of the 35th International Symposium on Microarchitecture</i> , Nov. 2002, pgs. 3-14.	
✓	A18	MICHAUD et al., "Data-Flow Prescheduling for Large Instruction Windows in Out-of-Order Processors", In <i>Proceedings of the Seventh International Symposium on High-Performance Computer Architecture</i> , Jan. 2001, pgs. 27-36.	
✓	A19	MOUDGILL et al., "Register Renaming and Dynamic Speculation: An Alternative Approach", In <i>Proceedings of the 26th International Symposium on Microarchitecture</i> , Dec. 1993, pgs. 202-213.	
✓	A20	PALACHARLA et al., "Complexity-Effective Superscalar Processors", In <i>Proceedings of the 24th Annual International Symposium on Computer Architecture</i> , June 1997, pgs. 206-218.	
✓	A21	RANGANATHAN et al., "Using Speculative Retirement and Larger Instruction Windows to Narrow the Performance Gap between Memory Consistency Models", In <i>Proceedings on the 9th Annual ACM Symposium on Parallel Algorithms and Architectures</i> , Jun. 1997, pgs. 199-210.	
✓	A22	ROTENBERG et al., "Trace Processors", In <i>Proceedings of the 30th International Symposium on Microarchitecture</i> , June 1997, pgs. 138-148.	
✓	A23	SMITH et al., "Implementation of Precise Interrupts in Pipelined Processors", In <i>Proceedings of the 12th Annual International Symposium on Computer Architecture</i> , June 1985, pgs. 36-44.	
✓	A24	SPRANGLE et al., "Increasing Processor Performance by Implementing Deeper Pipelines", In <i>Proceedings of the 29th Annual International Symposium on Computer Architecture</i> , May 2002, pgs. 25-34.	
✓	A25	STEFFAN et al., "A Scalable Approach to Thread-Level Speculation", In <i>Proceedings of the 27th Annual International Symposium on Computer Architecture</i> , June 2000, pgs. 1-12.	
✓	A26	TENDLER et al., "POWER4 System Microarchitecture", IBM J. Res. & Dev., vol. 46, no. 1, January 2002, pgs. 5-25,	
✓	A27	VIJAYAN et al., "Out-of-Order Commit Logic With Precise Exception Handling For Pipelined Processors", In <i>Poster in High Performance Computer Conference</i> , Dec. 2002.	
✓	A28	HWU et al., "Checkpoint Repair for Out-of-order Execution Machines", In <i>Proceedings of the 14th Annual International symposium on Computer architecture</i> , 1987, pgs. 18-26.	
✓	A29	YEAGER, "The MIPS R10000 Superscalar Microprocessor", IEEE Micro, April 1996, pgs. 28-40.	

Examiner Signature		Date Considered	
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